The following listing of the claims replaces all prior listings of the claims.

Listing of the Claims:

Claims 1-20 (Cancelled).

21. (Previously presented) A semiconductor circuit arrangement on a substrate comprising:

a doped semiconductor layer having a first conductivity type disposed on the substrate;

an insulating layer disposed on the doped semiconductor layer;

a charge storing layer configured for storing an electrical charge disposed on the insulating layer; and

at least one deep trench that penetrates through the charge storing layer and extends into the doped semiconductor layer.

22. (Previously presented) The semiconductor circuit arrangement of claim 21, where the charge storing layer is a conducting layer.

23. (Previously presented) The semiconductor circuit arrangement of claim 21, where the charge storing layer is an insulating layer.

24. (Previously presented) The semiconductor circuit arrangement of claim 21, where the at least one deep trench penetrates through the doped semiconductor layer into the substrate.

25. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a second doped semiconductor layer having a second conductivity type disposed between the substrate and the doped semiconductor layer, where the second conductivity type is opposite to the conductivity type of the doped semiconductor layer.

26. (Previously presented) The semiconductor circuit arrangement of claim 25, further comprising the at least one deep trench penetrating through the doped semiconductor layer and extending into the second doped layer.

27. (Previously presented) The semiconductor circuit arrangement of claim 25, further comprising the at least one deep trench penetrating through the doped semiconductor layer and the second semiconductor layer into the substrate.

28. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a conductive layer and a second insulating layer where the second insulating layer is disposed on the charge storing layer and the conductive layer is disposed on the second insulating layer.

29. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a shallow trench that is arranged in the doped semiconductor layer.

30. (Previously presented) The semiconductor circuit arrangement of claim 29, where the shallow trench does not penetrate through the charge storing layer and the insulating layer and the shallow trench extends about laterally symmetrical in all directions beyond an edge of the deep trench.

31. (Previously presented) The semiconductor circuit arrangement of claim 30, where the shallow trench extends laterally about 50 nm beyond the edge of the deep trench.

32. (Previously presented) The semiconductor circuit arrangement of claim 29, where the shallow trench contains an insulating material.

33. (Previously presented) The semiconductor circuit arrangement of claim 32, where the insulating material is polycrystalline silicon.

34. (Previously presented) The semiconductor circuit arrangement of claim 29, further comprising at least one shallow trench through which no deep trench penetrates.

35. (Previously presented) The semiconductor circuit arrangement of claim 34, where the semiconductor arrangement forms a logic circuit arrangement.

36. (Previously presented) The semiconductor circuit arrangement of claim 29, further comprising at least one shallow trench having the same depth as the deep trench.

37. (Previously presented) The semiconductor circuit arrangement of claim 29, further comprising at least one shallow trench where the deep trench penetrates through the bottom of the shallow trench.

38. (Previously presented) The semiconductor circuit arrangement of claim 37, where the semiconductor arrangement is a memory circuit arrangement.

39. (Previously presented) The semiconductor circuit arrangement of claim 29, where the electrically conductive layer extends at least partly over the shallow trench.

40. (Previously presented) The semiconductor circuit arrangement of claim 29, where the second electrically insulting layer extends at least partly over the shallow trench.

41. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a second charge storing layer disposed on the charge storing layer and the deep trench does not penetrate into the second charge storing layer.

42. (Previously presented) The semiconductor circuit arrangement of claim 41, further comprising an opening in the second charge storing layer above the deep trench.

43. (Previously presented) The semiconductor circuit arrangement of claim 42, where the edges of the opening are a smaller distance apart than the lateral edges of the deep trench.

44. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising an insulating material that fills the deep trench.

45. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising an insulating material disposed on the wall of the trench.

46. (Previously presented) The semiconductor circuit arrangement of claim 45, wherein the electrically insulating material on the wall of the trench is silicon dioxide.

47. (Previously presented) The semiconductor circuit arrangement of claim 45, where the trench is filled with an electrically conductive or semi-conductive material and the material is isolated from the trench wall with the electrically insulating material.

48. (Previously presented) The semiconductor circuit arrangement of claim 47, wherein the conductive or semi-conductive material is polysilicon.

49. (Previously presented) The semiconductor circuit arrangement of claim 21, further comprising a plurality of deep trenches each deep trench arranged next to one another in a transverse direction separating a plurality of charge storing layers arranged in the transverse direction.

50. (Previously presented) The semiconductor circuit arrangement of claim 49, wherein the plurality of deep trenches separate a plurality of memory cells arranged in the transverse direction, the combination of which forms a memory circuit.

51. (Previously presented) The semiconductor circuit arrangement of claim 50, wherein the plurality of memory cells form EEPROM memory cells or EEPROM flash memory cells.

52. (Withdrawn) A method for fabricating a semiconductor circuit arrangement comprising:

forming a doped semiconductor layer of a first conductivity type;

disposing an electrically insulating layer on the doped semiconductor layer;

disposing a charge storing layer on the electrically insulating layer; and

forming a deep trench that penetrates through the charge storing layer, the insulating layer and into the semiconductor layer.

53. (Withdrawn) The method of claim 52, further comprising

disposing a mask on the charge storage layer; and

forming the trench using the mask layer as a protection for the charge storage layer.

54. (Withdrawn) The method of claim 53, where the mask is a photoresist.

55. (Withdrawn) The method of claim 53, where the mask is a hard mask layer.

56. (Withdrawn) The method of claim 55, where the hard mask material is TEOS.

57. (Withdrawn) The method of claim 53, further comprising:

filling the deep trench with a filling material; and

etching back the filling material.

58. (Withdrawn) The method of claim 57, further comprising removing the mask after forming the trench and before filling the trench with the filling material.

59. (Withdrawn) The method of claim 57, further comprising forming an oxide liner on the inner wall of the trench where the oxide liner is formed before filling the trench.

60. (Withdrawn) The method of claim 57, where the etching back includes a CMP process.

61. (Withdrawn) The method of claim 57, further comprising:

etching back the filling material so that a region uncovered during the etching back process extends into a region where the semiconductor layer was formed; and

filling the uncovered region with a second filling material.

62. (Withdrawn) The method of claim 61, wherein the second filling material is an oxide.

63. (Withdrawn) The method of claim 52, further comprising:

forming a shallow trench in the doped semiconductor layer where the shallow trench is shallower and wider than the first trench;

filling the shallow trench with a third filling material; and

planarizing the filling material in the shallow trench, wherein the forming, filling and planarizing steps are performed before disposing the charge-storing layer.

64. (Withdrawn) The method of claim 63, where at least one shallow trench is arranged in a region where the deep trench penetrates the shallow trench.

65. (Withdrawn) The method of claim 63, wherein at least one shallow trench is arranged in a region where the deep trench does not penetrate the shallow trench.

66. (Withdrawn) The method claim 63, further comprising etching the third filling material such that the region uncovered during the etching extends into a region where the semiconductor layer was formed.

67. (Withdrawn) The method of claim 66, further comprising further filling the uncovered region with an insulating material.

68. (Withdrawn) The method of claim 66, further comprising further filling the uncovered region with a conducting material.

69. (Withdrawn) The method of claim 63, further comprising:

disposing at least one further conducting charge-storing layer adjoining the charge-storing layer; and

patterning the further charge-storing layer, where the patterning of the further charge storing layer forms a cutout that extends into the trench.

70. (Withdrawn) The method of claim 69, where the patterning is performed before disposing further layers on the further charge-storing layer.

71. (Withdrawn) The method of claim 63, further comprising:

disposing a further insulating charge storing layer adjoining the charge-storing layer; and

patterning the further charge storing layer, where the patterning of the further charge storing layer forms a cutout that extends into the deep trench.

72. (Withdrawn) The method of claim 71, where the patterning is performed before applying further layers on the further charge-storing layer.